deposited where the first portions of the gate oxide layer 156 were removed. Alternate dielectrics include high-k dielectrics, nitride stack dielectrics, and other known dielectrics. After depositing the first alternate dielectric, the wafer 150 is again masked and second portions of the gate oxide layer 156 are removed by etching. A second alternate dielectric is deposited where the second portions of the gate oxide layer were removed. Masking, etching, and alternate dielectric deposition is repeated until a desired number of different types of dielectric layers are deposited. An exemplary embodiment comprising different types of gate dielectrics is shown in FIG. 9, which comprises a high-k dielectric layer 160, a nitride stack dielectric layer 158, and a gate oxide layer 156.--

IN THE CLAIMS:

Claims 1 and 8 have been amended as follows:

1. (Amended) A wafer comprising:

a base layer;

an active layer formed on the base layer;

a gate dielectric layer formed on the active layer;

a conductive layer formed on the gate dielectric layer; and

a plurality of isolation regions formed in said wafer,

said wafer being divided into a plurality of first portions, second portions, and third portions;

said first portions comprise gate dielectric capacitors, said gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer; wherein the first electrode layer is formed from said active layer, the insulating

layer is formed from said gate dielectric layer, and the second electrode layer is formed from said conductive layer;

said second portions comprise first dummy structures, said first dummy structures comprise a first electrode layer and an insulating layer; wherein the first electrode layer of the first dummy structures is formed from said active layer and the insulating layer of the first dummy structures is formed from said gate dielectric layer, wherein said second portion does not contain said conductive layer; and

said third portions comprise second dummy structures, said second dummy structures comprise an insulating layer and a second electrode layer; wherein the insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from said conductive layer, wherein said third portion does not contain said active layer.

8. (Amended) The wafer of claim 1, further comprising a silicon electrode contacting an isolation region.

Please cancel claims 7 and 9.

Please add new claims 21 and 22 as follows:

--21. The wafer of claim 4, wherein said active layer comprises source/drain regions.

22. The wafer of claim 8, wherein said silicon electrode is an electrically isolated polysilicon electrode that contacts an isolation region of the second dummy pattern.--